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10/815,496	03/31/2004	Min Chih Hsuan	68,700-016	1166

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,496	HSUAN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) *4,23,24,26-35,40,59,60 and 62-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-15,17-22,25,36-39,41-44,46-51,53-58 and 61* is/are rejected.

7)☒ Claim(s) *9,16,45 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species 1, sub-species 1a, 2a, and 3a in the reply filed on 12/24/2005 is acknowledged. Non-elected claims 4, 23, 24, 26-35, 40, 59, 60, and 62-66 are withdrawn from consideration.

Claim Objections

Claim 9 is objected to because of the following informalities: in line 2, "from a distance" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 9, 37 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 37 recite the limitation "the body portion" in line 3 (claim 1) and line 2 (claim 37). Claims 1 and 37 recite the limitation "the top face" in line 4 (claim 1) and line 3 (claim 37). There is insufficient antecedent basis for these limitations in the claims.

Claims 9 and 45 recite the limitations "second distance" and "first distance" in lines 3-4 (claim 9) and line 3 (claim 45). There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 12, 18, 20, 22, 36-38, 48, 54, 56, and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (U.S. 2001/0006252).

Regarding claim 1, Kim et al. teaches a method of making a semiconductor package, comprising providing a semiconductor carrier comprising at least a first flexible appendage (left-hand side of carrier in Fig. 13) connected to a body portion (central portion of Fig. 13—the right-hand side is taken to be a second flexible appendage attached to the central body portion), each flexible appendage having a top face and a bottom face (upper and lower faces in Fig. 13), and the body portion having a top face and a bottom face (upper and lower faces in Fig. 13), a first semiconductor device and a second semiconductor device (**426** and the chip to its right in Fig. 13), each having a front face (bottom surface of device in Fig. 13) and a back face (top surface of device in Fig. 13), the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage; and forming a first fold in the first flexible appendage so that the back face of the first semiconductor device overlies the back face of the second semiconductor device (Fig. 14).

Regarding claim 37, Kim et al. teaches a semiconductor package comprising a semiconductor carrier comprising at least a first flexible appendage (left-hand of carrier

in Fig. 13) connected to a body portion (central portion of Fig. 13—the right-hand side is taken to be a second flexible appendage attached to the central body portion), each flexible appendage having a top face and a bottom face (upper and lower faces in Fig. 13), and the body portion having a top face and a bottom face (upper and lower faces in Fig. 13), a first semiconductor device and a second semiconductor device (**426** and the chip to its right in Fig. 13), each having a front face (bottom surface of device in Fig. 13) and a back face (top surface of device in Fig. 13), the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage, and the first flexible appendage having a first fold therein so that the back face of the first semiconductor device overlies the back face of the second semiconductor device (Fig. 14).

Regarding claims 2 and 38, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches forming a second fold in the first flexible appendage so that a portion of the bottom face of the first flexible appendage underlying the first semiconductor device also overlies the top face of the body portion (Fig. 14).

Regarding claims 12 and 48, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches bonding the first semiconductor device to the second semiconductor device with an adhesive (paragraph 0013).

Regarding claims 18 and 54, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that there is no spacer between the back face of the first semiconductor device and the back face of the second semiconductor device (Fig. 14).

Regarding claims 20 and 56, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that the body portion is flexible (note fold in body portion in Fig. 14).

Regarding claims 22 and 58, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that the carrier comprises a flexible circuit (paragraph 0008).

Regarding claim 36, Kim et al. teaches a method of making a semiconductor package as set forth in claim 1, and further teaches forming a fold in the body portion (Fig. 14).

Claims 1-3, 12, 17-20, 22, 37-39, 48, 53-56 and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Primavera et al. (U.S. 2002/0044423).

Regarding claim 1, Primavera et al. teaches a method of making a semiconductor package, comprising providing a semiconductor carrier comprising at least a first flexible appendage (**22** in Fig. 7A) connected to a body portion (**32** in Fig. 7A), each flexible appendage having a top face and a bottom face (upper and lower

faces in Fig. 7A), and the body portion having a top face and a bottom face (upper and lower faces in Fig. 7A), a first semiconductor device and a second semiconductor device (both labeled **10** in Fig. 7A), each having a front face (bottom surface of device in Fig. 7A) and a back face (top surface of device in Fig. 7A), the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage; and forming a first fold in the first flexible appendage so that the back face of the first semiconductor device overlies the back face of the second semiconductor device (Fig. 7B).

Regarding claim 37, Primavera et al. teaches a semiconductor package comprising a semiconductor carrier comprising at least a first flexible appendage (**22** in Fig. 7A) connected to a body portion (**32** in Fig. 7A), each flexible appendage having a top face and a bottom face (upper and lower faces in Fig. 7A), and the body portion having a top face and a bottom face (upper and lower faces in Fig. 7A), a first semiconductor device and a second semiconductor device (both labeled **10** in Fig. 7A), each having a front face (bottom surface of device in Fig. 7A) and a back face (top surface of device in Fig. 7A), the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage, and the first flexible appendage having a first fold therein so that the back face of the first semiconductor device overlies the back face of the second semiconductor device (Fig. 7B).

Regarding claims 2 and 38, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches forming a second fold in the first flexible appendage so that a portion of the bottom face of the first flexible appendage underlying the first semiconductor device also overlies the top face of the body portion (Fig. 7B).

Regarding claims 3 and 39, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 2 and a semiconductor package as set forth in claim 38, and further teaches bonding a semiconductor device to the body portion prior to forming the second fold, and wherein the first semiconductor device overlies the semiconductor device bonded to the body portion (Fig. 20 shows bottom chip **10** secured to rigid carrier **70** of the body portion; paragraph 0061).

Regarding claims 12 and 48, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches bonding the first semiconductor device to the second semiconductor device with an adhesive (**74** in Fig. 20; paragraph 0061).

Regarding claims 17 and 53, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that at least one of the first and second semiconductor devices further comprises an electrically conductive bump connecting the semiconductor device to the first flexible appendage (Figs. 7A-7B).

Regarding claims 18 and 54, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set

forth in claim 37, and further teaches that there is no spacer between the back face of the first semiconductor device and the back face of the second semiconductor device (Fig. 7B).

Regarding claims 19 and 55, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches an electrical connector extending from the body portion (solder connections in Figs. 7A-7B).

Regarding claims 20 and 56, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that the body portion is flexible (paragraphs 0044, 0046).

Regarding claims 22 and 58, Primavera et al. teaches a method of making a semiconductor package as set forth in claim 1 and a semiconductor package as set forth in claim 37, and further teaches that the carrier comprises a flexible circuit (paragraph 0046).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8, 10, 11, 13, 41-44, 46, 47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al. (U.S. 2002/0044423) in view of Shibata et al. (U.S. 2002/0127773).

Regarding claims 5 and 41, Primavera et al. teaches the method of claim 1 and the packaging of claim 37 (note 35 U.S.C. 102(b) rejection above), but does not teach that the first semiconductor device further comprises a first alignment key and the second semiconductor device further comprises a second alignment key matable with the first alignment key, and mating the first alignment key with the second alignment key when the back face of the first semiconductor device overlies the back face of the second semiconductor device.

Shibata et al. teaches two semiconductor devices (**20** and **10** in Fig. 1a), one of which comprises a first alignment key (bumps **22** in Fig. 1a), the other of which comprises a second alignment key (bumps **12** in Fig. 1a), and joining the semiconductor devices so that the alignment keys mate (Fig. 1c).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Primavera et al. and Shibata et al. by mating the two semiconductor devices face-to-face, as taught by Primavera et al., and further forming alignment keys (bumps) that mate together with the devices are joined, as taught by Shibata et al. The motivation for doing so at the time of the invention would have been to facilitate joining the devices, as taught by Shibata et al. (paragraph 0024).

Regarding claims 6, 7, 42, and 43, Primavera et al. and Shibata et al. together teach the method of claim 5 and the packaging of claim 41. Shibata et al. further

teaches forming both of the first alignment key and the second alignment key by depositing a raised feature on the back face of one of the first semiconductor device and second semiconductor device (Fig. 1a; paragraph 0022).

Regarding claims 8 and 44, Primavera et al. and Shibata et al. together teach the method of claim 5 and the packaging of claim 41. Shibata et al. further teaches that the first alignment key comprises a raised feature spaced a distance from a side edge of the first semiconductor device (Fig. 1a).

Regarding claims 10, 11, 46, and 47, Primavera et al. and Shibata et al. together teach the method of claim 5 and the packaging of claim 41. Shibata et al. further teaches that the first alignment key comprises a raised feature positioned near a side edge of the first semiconductor device and the second alignment key comprises a raised feature spaced a distance from a side edge of the second semiconductor device (Fig. 1a).

Regarding claims 13 and 49, Primavera et al. and Shibata et al. together teach the method of claim 5 and the packaging of claim 42. Shibata et al. further teaches depositing an electric insulation layer on each of the first and second semiconductor devices and thereafter forming the first alignment key on one of the first and second semiconductor devices and forming the second alignment key on the other of the first and second semiconductor devices (paragraphs 0021-0022).

Claims 14 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al. (U.S. 2002/0044423) in view of Shibata et al. (U.S. 2002/0127773)

as applied to claims 13 and 49 above, and further in view of Tago et al. (U.S. 2002/0090756).

Regarding claims 14 and 50, Primavera et al. and Shibata et al. together teach the method and packaging of claims 13 and 49 (note 35 U.S.C. 103(a) rejection above), but do not teach that the forming of each of the first and second alignment keys comprises depositing a material comprising copper.

Tago et al. teaches a method of bonding two semiconductor devices using alignment keys (bumps) comprising CuSn (paragraphs 0063-0068).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method and packaging taught by Primavera et al. and Shibata et al. together, and form the alignment keys of a material comprising copper, as taught by Tago et al. The motivation for doing so at the time of the invention is that Tago et al. demonstrates that CuSn forms a strong bond with itself to join two semiconductors together (paragraphs 0063-0068).

Claims 21 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al. (U.S. 2002/0044423) in view of Kamei et al (U.S. 2001/0008306).

Regarding claims 21 and 57, Primavera et al. teaches the method and packaging of claims 1 and 37 (note 35 U.S.C. 102(b) rejection above), but does not teach that the body portion comprises a ceramic.

Kamei et al. teaches a semiconductor package having a body portion and at least a first flexible appendage, the body portion comprising a ceramic (paragraph 0040;

72 in Fig. 2). The ceramic body portion ensures a leveling effect of the folded laminate (paragraph 0040).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method and packaging taught by Primavera et al. and form the body portion of a material that comprises a ceramic in order to ensure a leveling effect of the folded laminate, as expressly taught by Kamei et al.

Claims 15 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al. (U.S. 2002/0044423) in view of Shibata et al. (U.S. 2002/0127773) as applied to claims 13 and 49 above, and further in view of D'Amato et al. (U.S. 2004/0089880).

Regarding claims 15 and 51, Primavera et al. and Shibata et al. together teach the method and packaging of claims 13 and 49 (note 35 U.S.C. 103(a) rejection above), but do not teach that at least one of the first and second alignment keys comprises a bump having a ring shape.

D'Amato et al. teaches a ring-shaped alignment key for aligning a semiconductor wafer to a substrate (Figs. 10, 11a, and 11b; paragraph 0049). The mating alignment key is centered within the ring-shaped alignment key, aiding in alignment (paragraph 0049).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method or packaging taught by Primavera et al. and Shibata et al. together, and further make one of the alignment keys ring-shaped, so that the mating alignment key can be easily centered, as taught by D'Amato et al.

Claims 25 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al. (U.S. 2002/0044423) in view of Ma (U.S. 6,808,955).

Regarding claims 25 and 61, Primavera et al. teaches the method of claim 1 and the packaging of claim 37 (note 35 U.S.C. 102(b) rejection above), but does not teach that at least one of the first and second semiconductor devices comprises a micro-electromechanical (MEMS) device.

Ma teaches a method of packaging a micro-electromechanical device by joining two wafers face-to-face (Fig. 7; column 3, lines 25-42). This method improves product performance and decreases manufacturing costs (paragraph bridging columns 3 and 4).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method or packaging taught by Primavera et al., and further incorporate a MEMS device onto one of the semiconductor devices, since Ma teaches a that packaging a MEMS device face-to-face with another semiconductor wafer can improve product performance and decrease manufacturing costs.

Allowable Subject Matter

Claims 9, 16, 45, and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 9 and 45, prior art does not teach or suggest, in combination with the other claimed limitations, that the second alignment key comprises a raised

feature and is spaced a distance from a side edge of the second semiconductor device a distance that is shorter than the distance the first alignment key is spaced from the edge of the first semiconductor device. Shibata et al. teaches that the distances between the edges of the semiconductor devices and the alignment keys are equal, and there is no motivation to combine this teaching with other relevant prior art to arrive at the invention as claimed in claims 9 and 45.

Regarding claims 16 and 52, prior art does not teach or suggest, in combination with the other claimed limitations, the combination of one ring-shaped alignment key and one L-shaped alignment key.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nicewarner, Jr., et al. (U.S. 5,646,446) teaches a packaging having a flexible appendage that folds to join two semiconductor devices face-to-face.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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